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The Impact of Gate-Driver Parameters Variation and Device Degradation in the PV-Inverter Lifetime

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Abstract— This paper introduces a reliability-oriented design tool for a new generation of grid connected PV-inverters. The proposed design tool consists of a real field Mission Profile (MP) model (for one year operation in USA-Arizona), a PV-panel model, a grid connected PV-inverter model, an Electro-Thermal model and the lifetime model of the power semiconductor devices. A simulation model able to consider a one year real field operation conditions (solar irradiance and ambient temperature) is developed. Thus, one year estimation of the converter devices thermal loading distribution is achieved and is further used as an input to a lifetime model. The proposed reliability oriented design tool is used to study the impact of MP-variation, Gate-Driver (GD) parameters variation and device degradation in the PV-inverter lifetime. The obtained results indicate that in order to improve the accuracy of the lifetime estimation it is crucial to consider also the device degradation feedback. Moreover the MP of the field where the PV-inverter is operating and the GD-parameters selection has an important impact in the converter reliability and it should be considered from the design stage to better optimize the converter design margin.

Keywords— mission profile variation, gate-driver parameters variation, device degradation feedback, SiC-devices;

I. INTRODUCTION

The converter availability in PV-system applications is the most important aspect and it depends on the component reliability, efficiency and its maintenance [1, 2]. Moreover, field experiences in renewables reveal that PV-inverters are responsible for more than one-third (37 %) of the unscheduled maintenance and more than a half (59%) of the associated cost during five years of operation of a 3.5 MW PV-plant [3]. Therefore, highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs [4, 5].

The design of high reliable PV-inverters under constrained cost is a great challenge to be overcome. Switching devices are one of the reliability-critical components, which will exposure to long-term mission profiles of solar irradiance and ambient temperature. Among other kind of stresses, peak temperature and temperature variations are the most critical ones. Therefore, a reliability-oriented design tool is highly expected to perform the long-term (e.g. one year) electro-thermal and then the reliability aspect analysis of switching devices in PV-inverters. Even if the typical design target of lifetime for PV-

systems is around 20 years, there is a discrepancy between the lifetime of the PV-inverter (5-10 years) and the PV-panel (20-25 years). The system reliability can be improved by replacing devices before their failure [5, 6]. Great variations of the PV-inverters lifetime are encountered due to the Mission Profile (MP) and Gate-Driver (GD) parameters variations. Therefore, in order to achieve reliability improvement and cost reduction of the PV-technology, it is of major importance to predict the lifetime of the PV-inverter, according with the operating conditions.

The loading stress (e.g. thermal loading of devices, cyclic load, voltage etc.) of the PV-inverter devices is a consequence of the MP and of the GD-parameters variations (gate resistance and gate voltage presented in Fig. 1). Moreover, the device strength model is a consequence of any physical properties (e.g. hardness, melting point, adhesion, etc.) which defines how much loading the component can withstand [2]. A component failure occurs when the applied stress exceeds the designed strength. By analyzing the overlap area between the stress-strength distributions, the probability of failure can be obtained (Fig. 2). Therefore, stress and strength, are two of the most important factors which have to be considered for lifetime estimation of PV-inverters.

The knowledge gained from the field data and simulations of high power devices concluded that the temperature is one of the most important stressor which involves failures in power semiconductor devices. For each 10°C increase in temperature the failure rate is almost doubled.

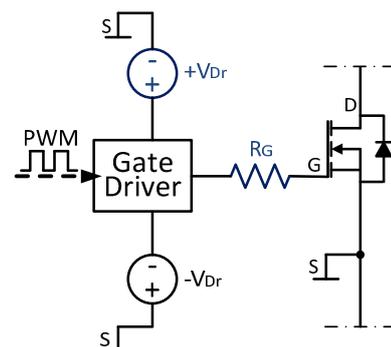


Fig. 1. Gate-Driver schematic emphasizing the main parameters in terms of gate-voltage V_G and gate-resistance R_G

Therefore, the temperature variation of the semiconductor devices plays a key role in the robustness-design and reliability of power-electronics converters. This factor has a major impact on the power converters used in renewable-energy systems, like solar-energy applications, due to the fluctuating nature of the MP (solar irradiance). The introduced converter current changes cause device junction temperature variations (due to the power loss dissipation) that significantly reduce the reliability of the semiconductor-devices.

The conduction and switching losses of the device (MOSFET) are influenced by the gate-driver (Fig. 1) parameters in terms of gate-voltage (V_{GS}) and gate-resistance (R_G). Moreover, different GD-operating conditions may influence the device power-losses, the temperature and implicitly the device reliability.

By achieving a more constant power-losses dissipation (in the semiconductor-device), the junction temperature can be kept constant, thus enhancing the reliability of power semiconductor devices. Therefore, a gate-driver able of controlling the device power-loss dissipation is of great interest in order to enhance the reliability of the power-electronics devices used in grid-connected PV-inverter applications. Thus, it is of major importance to study the GD-parameters (V_{GS} and R_G) variation impact on PV-inverter devices lifetime considering the device intrinsic limits in terms of gate-oxide breakdown, thermal runaway, gate-ringing and PWM limit.

Moreover, the MP-variation and GD-operating conditions (GDs1 and GDs2) will have an impact in the device degradation (D1 and D2) involving different failure distribution as shown in Fig. 2. If the stress has the distribution according to Fig. 2, the converter devices have a lower lifetime if they are operating under GDs2 (which involves D2) when compared with GDs1 (which involves D1).

This paper proposes a reliability oriented design tool for the new generation of grid connected PV-inverter in order to study

the impact of mission profile (MP) variation, gate driver parameters variations (GD) and device degradation (D) in the PV-inverter devices lifetime.

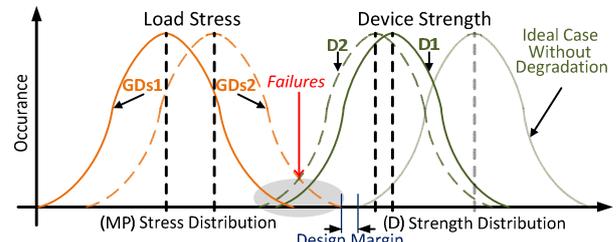


Fig. 2. Stress-Strength analysis emphasize the overstress failure due to GDs variation

II. PROPOSED RELIABILITY ORIENTED-DESIGN TOOL

Referring to Fig. 3, the proposed design tool consists of a real field mission profile model, a PV-panel model, a grid-connected PV-inverter model, an Electro-Thermal model and a Lifetime model.

The involved parameters emphasized in Fig. 3 are as follows: G - solar irradiance, T_a - ambient temperature, $V_{DC-Link}$ - DC-Link voltage, I_{conv} - converter output current, I_M - MOSFET drain current, I_D - freewheeling diode current, V_{DC} - device off-state voltage, F_{sw} - switching frequency of the device, $Z_{th_device/grease/heatsink}$ - junction to case/grease/heatsink thermal impedance, T_j - device junction temperature, V_G - gate voltage, R_G - gate resistance, T_C - case temperature of the device, D - device degradation (aging). A description of each model is presented as follows:

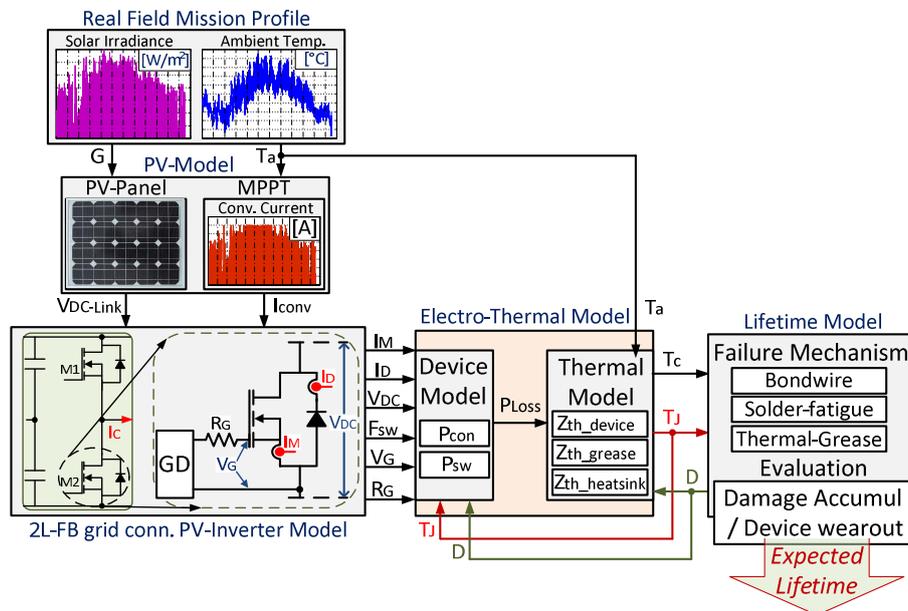


Fig. 3. Proposed reliability-oriented design structure for the new generation of grid connected PV-inverters

A. Real Field Mission Profile Model

The proposed design-tool presented in Fig. 3 considers the mission profile (MP) of the real field where the converter will operate. In order to study the impact on the PV-inverter devices reliability, the mission profile model is developed based on one-year measurements of solar irradiance (G) and ambient temperature (T_a) of harsh environment conditions from Arizona, USA (Fig. 10). The sampling time of the measured data is one minute. Thus, a realistic loading of the converter devices can be achieved, taking into account short time and longer time variations.

B. PV-Panel Model

The PV-panel model estimates the output current and voltage by considering as input the solar irradiance (G) and the ambient temperature (T_a) from the MP model. The model considers the configuration of the PV-Panel connection and finally estimates the PV-inverter DC-Link voltage and current variations. Considering the Maximum Power Point Tracking (MPPT) strategy, the references for the converter voltage and current are obtained.

C. PV-Inverter Model

The proposed PV-system, depicted in Fig. 4, consists of a 25 kVA SiC-based 2-Level Full Bridge (2L-FB) inverter connected to three-phase grid through a passive LCL-filter. Table I presents the PV-system design ratings. Fig. 4 also introduces the main control blocks, which are used to achieve the desired converter functionalities. The PV-inverter model receives as input the reference current and voltage from the MPPT. By considering the input, the model estimates the realistic device (MOSFET and Diode) loading current (I_M or I_D) and the voltage variations (off-state voltage V_{DC}). A more detailed description of the grid connected PV-inverter control design has been presented in [7].

TABLE I. PV-SYSTEM DESIGN RATINGS

3L-FB VSI PV-inverter Specifications			
Rated power	S = 25 kVA		
Conv. Output phase voltage	$V_N = 230$ V (RMS) (325 V peak)		
Max. Output current	$I_{max} = 37$ A (RMS) (52 A peak)		
Max. DC-link Voltage	$V_{DC-max} = 1000$ V		
Switching Frequency	$f_{sw} = 50$ kHz		
Thermal Impedance Values			
Heatsink	$R_{th} = 0.13$ [K/W]	$\tau = 570$ [s]	
Thermal Grease	$R_{th} = 0.0059$ [K/W]	$\tau = 1.3$ [s]	
LCL-Filter Parameters			
Parameters	$L_C = 4e-4$ H	$L_g = 1.5e-4$ H	$C_f = 0.4$ μ F
Device Characteristics			
Device type	CREE MOSFET Module (CCS050M12CM2)		
PV-Panel Characteristics-Connection			
PV-Panel Type	ET Black Module (ET-M660250BB)		
Conn. Type	Series=24	Parallel=3	

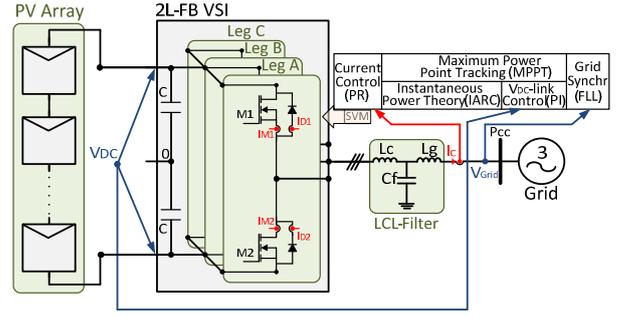


Fig. 4. Three phase grid connected 2L-FB PV-inverter application

D. Electro-Thermal Model

The proposed model aims at estimating the junction and case temperature for the new generation of power electronics devices. The input signals in the model are: the realistic device (MOSFET and Diode) loading current (I_M or I_D) and voltage variations (off-state voltage V_{DC}), the switching frequency (f_{sw}), the ambient temperature (T_a), the gate-driver operation point (V_G and R_G) and the device degradation level (D). According to Fig. 5, three types of models are involved in the electro-thermal analysis: the device model, the power loss model and the thermal model. The device model estimates the voltage drop across the device and the switching energies as a function of the current, the off-state blocking voltage and the junction temperature. Furthermore, the estimated parameters and the switching frequency will be used into the power loss P_{Loss} model where the instantaneous conduction and switching losses of the device are calculated. The total losses (P_{total_loss}) and the ambient temperature (T_a) are fed into the thermal model which estimates the device case temperature (T_c) and the junction temperature (T_j). Moreover, by providing the junction temperature as a feedback to the device model, the temperature impact in the losses is also considered. Finally, the device degradation (D) and gate-driving strategy (GDs) influence into the junction and the case temperature estimation are also included as follows:

- Device degradation (analysed in section II.E) in terms of junction-to-case thermal impedance degradation (given by solder fatigue) and on-state resistance degradation (given by bond-wire lift-off).
- Gate-derive strategy impact in terms of gate-voltage (V_G) and gate-resistance (R_G) variations.

By combining the Shockley model of the diode [8] with the resistance model, an accurate estimation of the device parameters in the whole working area has been achieved. The junction and case temperature estimation of the device (MOSFET and Diode) has been performed by implementing the proposed electro-thermal model according with [9].

The device model validation has been achieved by comparing the obtained simulation results with the experimental values, when applying the same operating conditions. Three gate driving strategies are mainly studied: GDs1 ($V_{GS}=20$ V and $R_G=7$ Ω), GDs2 ($V_{GS}=15$ V and $R_G=20$ Ω) and GDs3 ($V_{GS}=10$ V and $R_G=70$ Ω).

Fig. 6 (a) presents the MOSFET V_{DS} on-state voltage drop estimation, when the current is increased from 0 A to 50 A, for gate voltage values of 20 V, 15 V and 10 V. Moreover the temperature impact is also considered for 25°C and 150°C. Fig. 6 (b) shows the estimated switching energies for

MOSFET (E_{on} and E_{off}), when the current is increased from 0 to 50A and the gate resistance values are 7 Ω , 20 Ω and 70 Ω . Finally, the diode V_F -forward voltage drop is also emphasized (Fig. 6 (c)) for the same current values and junction temperature of 25°C and 150°C.

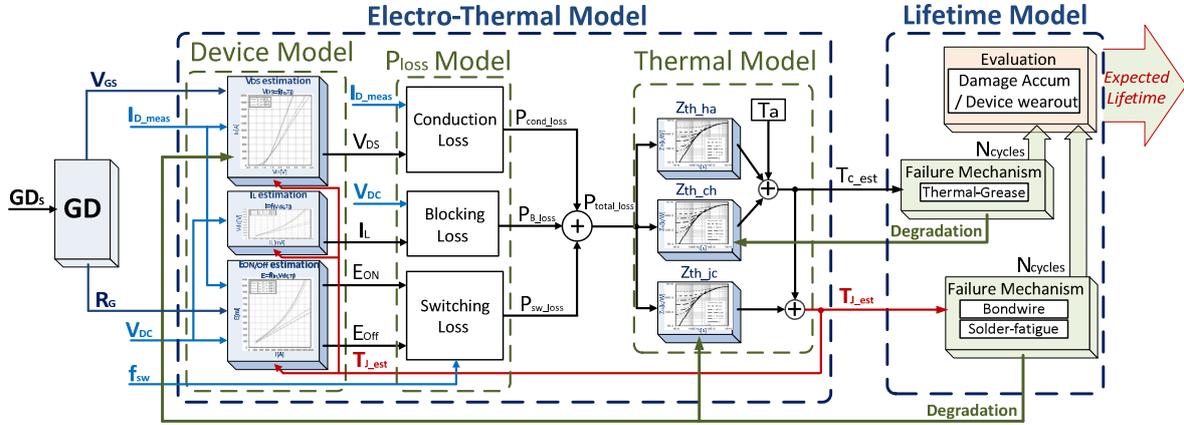


Fig. 5. Proposed Electro-Thermal model structure for device junction and case temperature estimation

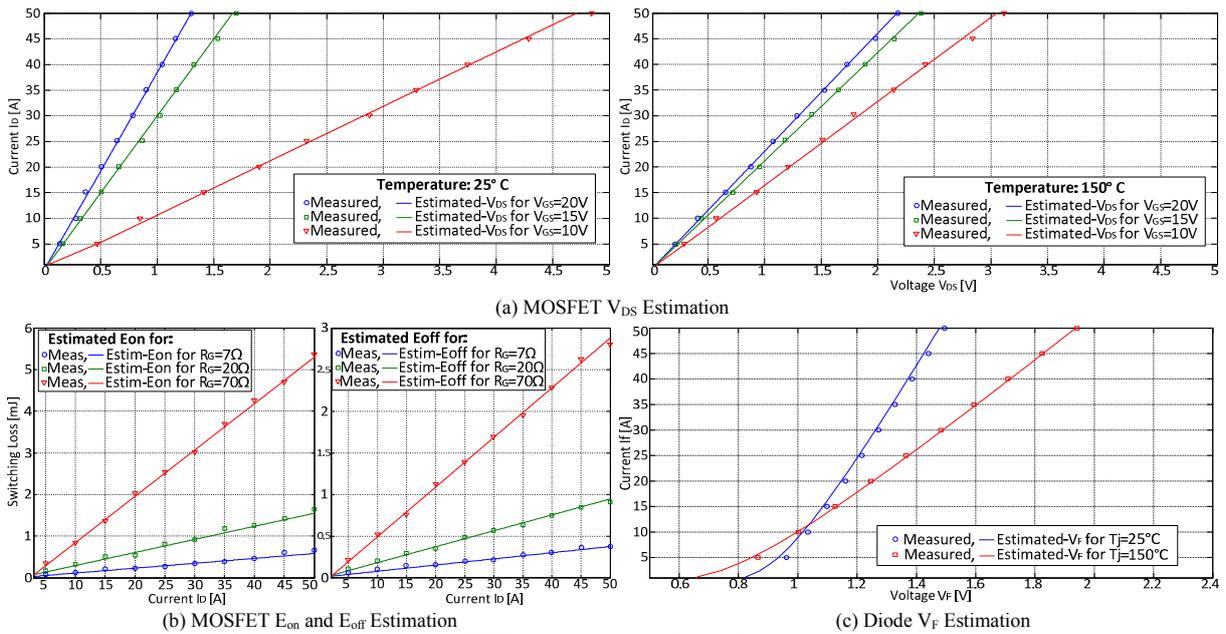


Fig. 6. Estimation of MOSFET voltage drop (a), MOSFET switching energies E_{on} and E_{off} (b) and of Diode voltage drop (c) when the current is increased from 0A to 50A and the junction temperature is increasing from 25°C to 150°C

E. Device Lifetime Model

Since the intensive work on the power-cycling testing of SiC power-devices is still undergoing, well-developed degradation models and lifetime models are unavailable at present for the analysed SiC power-module. To demonstrate the procedures of the proposed design-tool, the state-of-the-art lifetime models of Si-IGBT modules are applied for the SiC-devices.

Therefore, the results of the lifetime evaluation could be interpreted for relative-evaluation and for comparison only. A more relevant lifetime evaluation is upon the replacement by the specific lifetime models of the SiC power-modules in the future. Nevertheless, the procedures in the proposed design tool are still valid. There are various failures modes for power-electronics devices.

The power-electronics devices reliability can be analysed and studied from two perspectives:

- Semiconductor-chip reliability.
- Device-packaging reliability.

When dealing with silicon carbide (SiC) semiconductor chip, one of the main reliability problems was due to the gate-oxide break-down. As a wide-bandgap semiconductor-material, SiC has excellent properties for high breakdown electric-field and high thermal-conductivity, making it a good candidate for high temperature, high frequency and high power applications.

However, it has long been a common believe that the gate-oxide grown on SiC-semiconductor is not reliable enough, especially at high temperature where SiC-devices are expected to excel [10-13].

Based on a literature survey, nowadays it can be stated that the thermally-grown gate-oxide on SiC-semiconductor is intrinsically reliable even at high temperature as 375°C [14].

Fig. 7 shows that with the current SiC-processing technology it can be achieved a high reliability of the gate-oxide breakdown. According to Fig. 7, for a $V_{GS}=20$ V a time to failure of $1e+07$ hours lifetime is achieved [15]. Given such a promising result, the whole breakdown reliability question for gate-oxide on SiC-material is no longer a problem. Therefore, the proposed paper will mainly focus on the packaging-related reliability studies.

Two of the most commonly observed (packaging related) failures are die-attach solder-fatigue and bond-wire damage [16-18]. They are both caused by temperature cycling during operation and Thermal Expansion Coefficient (CTE) mismatch between adjacent layers. Bond-wire damage is more pronounced after die-attach solder is seriously degraded [19, 20]. The solder fatigue will not destroy the device directly, whereas the end of life failure is bond-wire damage related [16, 20]. Therefore, device junction temperature (mean junction temperature T_j and junction temperature variation ΔT_j) is one of the critical parameters required for lifetime estimation.

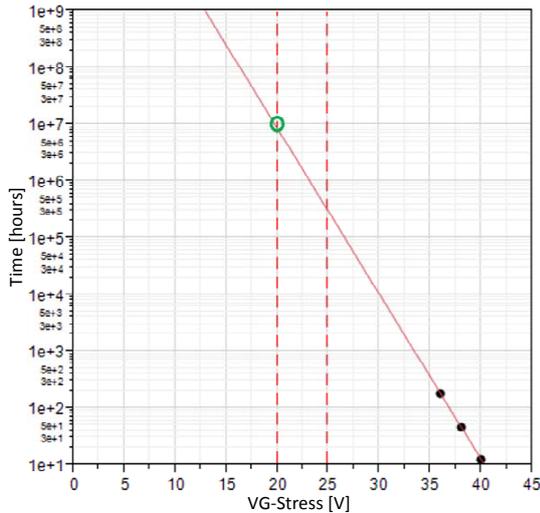


Fig. 7. Gate-Oxide lifetime of 20A CREE MOSFET [15]

The failure criteria are defined based on previous research works [16], [21] and [22]. Thus, [16] and [21] claims that 10% increase of on-state voltage V_{DS} indicates the bond-wire damage. Moreover, [16] and [22] suggested that a 40% increase of junction to case thermal resistance $R_{th,jc}$ indicates the solder-fatigue failure. The $R_{th,jc}$ has a linear degradation behaviour with lifetime level while V_{DS} is mainly changing in the last stage of the lifetime (from 80% to 100%) [16]. Table II presents the degradation impact on $R_{th,jc}$ and V_{DS} with the lifetime level.

As shown in Fig. 5, the degradation (of $R_{th,jc}$ and V_{DS}) is provided as a feedback in the electro-thermal model, thus the degradation impact in the losses is also included. As a trade-off between accuracy and simulation time, five degradation levels are included according to Table II.

TABLE II. DEVICE DEGRADATION WITH LIFETIME-LEVEL

	Lifetime level:	Degradation-Aging Impact	
		Normalized $R_{th,jc}$	Normalized V_{DS}
1.	0-20%	1	1
2.	20%-40%	1.1	1
3.	40%-60%	1.2	1.01
4.	60%-80%	1.3	1.03
5.	80%-100%	1.4	1.1

The lifetime model (SKiM 63) proposed by Semikron is used for the device lifetime estimation [23]. The model uses as a base-line the LESIT lifetime model [21]. Moreover, the dependency on the: wire bond aspect ratio (ar), load pulse duration (t_{on}) and on the freewheeling diode chip thickness (f_{Diode}) are also considered. The lifetime equation which expresses the number of cycles to failure (N_f) is described by (1).

$$N_f = A \cdot \Delta T_j^\alpha \cdot \exp\left(\frac{E_a}{k_B \cdot T_{jm}}\right) \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{on}^\gamma}{C + 1}\right) \cdot f_D \quad (1)$$

Moreover, Table III presents the parameters values used in the model.

TABLE III. DEVICE LIFETIME PARAMETERS

Parameter:	Value:
Technology factor: A	3.4368e+14
A	-4.923
Activation energy: E_a [eV]	0.06606
Bond-wire aspect ratio: ar	0.31
β_0	1.942
β_1	-9.012e-3
C	1.434
\square	-1.208
Cycling period: t_{on} [s]	0.07
Diode chip-thickness: f_{Diode}	0.6204

III. GATE DRIVER PARAMETERS IMPACT ON PV-INVERTER DEVICES POWER LOSSES

The conduction and switching losses of the device are influenced by the gate driver (GD) parameters in terms of gate-voltage (V_{GS}) and gate-resistance (R_G). In order to study the GD-parameters variation impact on the PV-inverter devices lifetime, it is very important to determine their range. Considering the device intrinsic limits emphasized in Fig. 8 (gate-oxide breakdown, thermal runaway, gate-ringing and PWM limit) the allowed V_{GS} and R_G range are determined as:

- The minimum turn-on gate voltage $V_{GS_min}=10$ V is chosen from the typical output characteristic given from the datasheet in order to avoid the thermal runaway of the device [24].
- The maximum turn-on gate voltage $V_{GS_max}=20$ V is provided in the datasheet in order to avoid the gate-oxide breakdown.
- The minimum allowed gate resistance $R_{G_min}=7$ Ω has been determined experimentally in order to avoid the gate ringing.
- The maximum allowed gate resistance $R_{G_max}=70$ Ω is determined by considering the PWM-limit.

The safe operating area of the device (Fig. 8) lies between the minimum and maximum allowed gate resistance ($R_{G_min}=7$ Ω , $R_{G_max}=70$ Ω) and gate-source voltage ($V_{GS_min}=10$ V, $V_{GS_max}=20$ V). With respect to the device power-losses, two main gate-driving operation points can be distinguished: the lowest loss operating point (V_{GS_max} and R_{G_min}) and the highest loss operating point (V_{GS_min} and R_{G_max}), respectively.

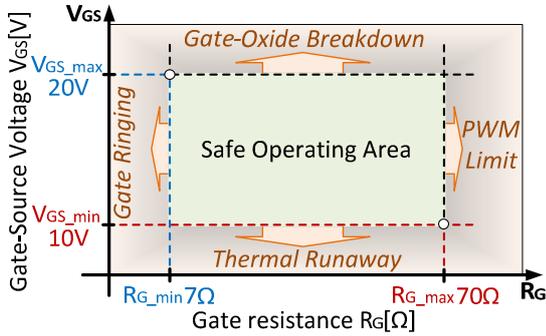


Fig. 8. Gate Driver parameters gate-voltage V_G and gate-resistance R_G maximum allowed range

In order to study the GD-parameters variation impact on the reliability of the proposed PV-inverter, six GD operating points have been proposed as follows: GDs1 ($V_{GS1}=20$ V and $R_{G1}=7$ Ω), GDs2 ($V_{GS2}=17$ V and $R_{G2}=12$ Ω), GDs3 ($V_{GS3}=15$ V and $R_{G3}=20$ Ω), GDs4 ($V_{GS4}=14$ V and $R_{G4}=35$ Ω), GDs5 ($V_{GS5}=12$ V and $R_{G5}=55$ Ω) and GDs6 ($V_{GS6}=10$ V and $R_{G6}=70$ Ω).

Fig. 9 presents the converter power losses variation when the current is increased from 0 to 50A for the proposed GD operating points. It can be clearly seen that according with the driving parameters, the losses can increase drastically.

Therefore, it is of major importance to study the impact of GD-parameters variation on the inverter devices lifetime.

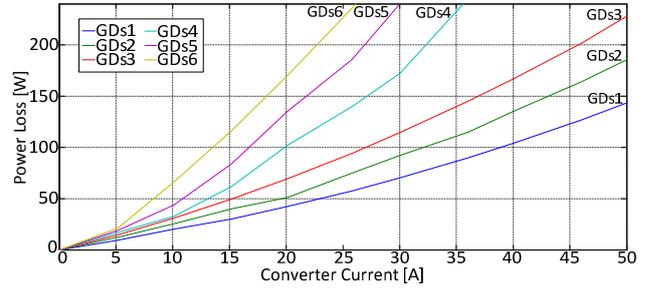


Fig. 9. Gate driver parameters impact in converter power losses when the following strategies are considered: GDs1 ($V_{GS1}=20$ V, $R_{G1}=7$ Ω), GDs2 ($V_{GS2}=17$ V, $R_{G2}=12$ Ω), GDs3 ($V_{GS3}=15$ V, $R_{G3}=20$ Ω), GDs4 ($V_{GS4}=14$ V, $R_{G4}=35$ Ω), GDs5 ($V_{GS5}=12$ V, $R_{G5}=55$ Ω) and GDs6 ($V_{GS6}=10$ V, $R_{G6}=70$ Ω).

IV. LIFETIME ANALYSIS OF PV-INVERTER DEVICES

The proposed reliability oriented design tool is used to study the impact of the MP-variation, GD-parameters variation and device aging-degradation in the PV-Inverter devices lifetime. The process flow is further explained by considering the GDs presented in section III.

The simulation model is using as an input the one year MP from Arizona, USA: solar irradiance G (Fig. 10 (a)) and ambient temperature T_a (Fig. 10 (b)).

The obtained simulation results are presented in Fig. 11 and shows the realistic load current of the converter (for one year operation in USA Fig. 11 (a)) due to the real field mission profile applied as an input to the model (Fig. 10). Moreover, the thermal loading distribution of the converter devices (MOSFET and Diode) in terms of junction and case temperature (Fig. 11 (b)) has been estimated.

The obtained one-year thermal loading distribution of the converter devices in terms of mean junction temperature (T_j) and junction temperature variation (ΔT_j) has been further used as an input to the lifetime model presented in section II.e. Furthermore, the total device accumulated damage has been determined according with Miner's rule, with and without considering the device degradation feedback loop in the model. The expected PV-inverter devices lifetime is predicted considering that the device fails when the accumulated damage is 1. The MP and device degradation impact in PV-inverter lifetime considering the above mentioned GD strategies is presented in Table IV.

According to the obtained results (Table IV), depending on the GDs which is used the device degradation feedback has an impact of 28.2 to 34.1 % in the PV-inverter lifetime estimation accuracy. In order to have correct lifetime estimation it is crucial to consider also the device degradation feedback loop in the simulation model.

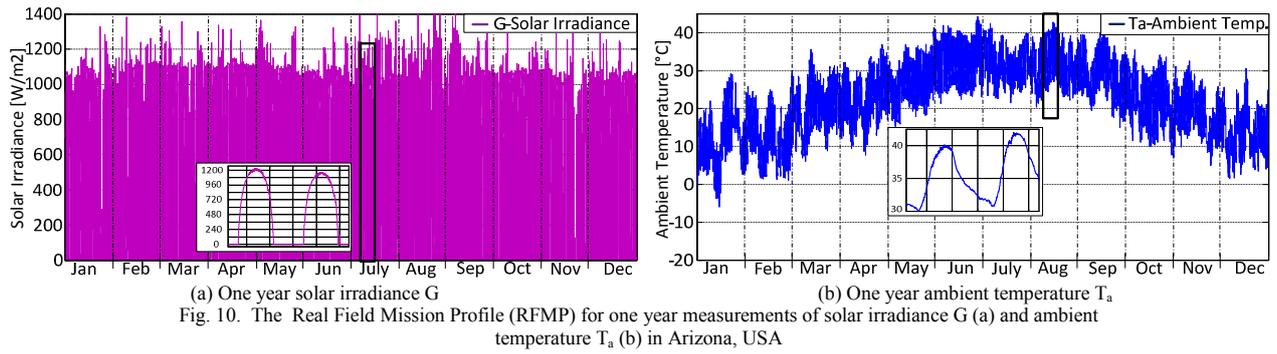


Fig. 10. The Real Field Mission Profile (RFMP) for one year measurements of solar irradiance G (a) and ambient temperature T_a (b) in Arizona, USA

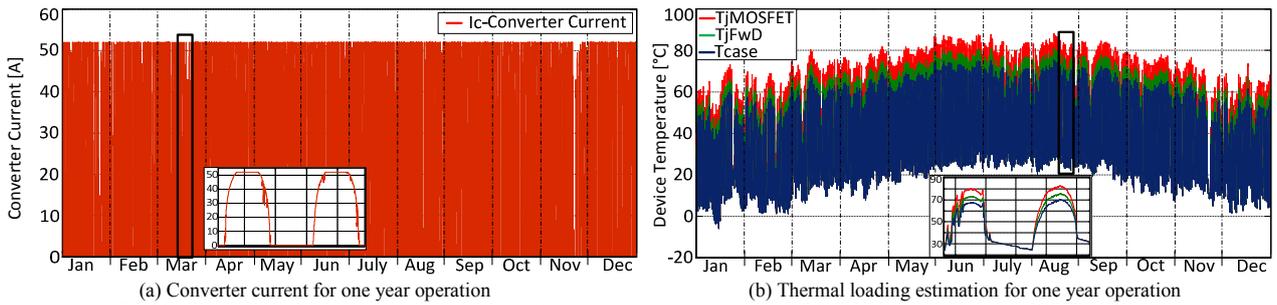


Fig. 11. The realistic PV-inverter loading current (a) and thermal loading estimation (b) of the inverter devices (MOSFET, Diode) for one year operation in Arizona, USA

The conduction and switching losses of the device are influenced by the gate-driver (GD) parameters in terms of gate-voltage (V_{GS}) and gate-resistance (R_G). Therefore, it is of major importance to study the impact of GD-parameters variation on the inverter devices' lifetime.

By considering the above mentioned process flow, the proposed tool is used to study the impact of GD-parameters variation in PV-inverter devices' lifetime considering also the MP-variation.

The obtained results presented in Fig. 12, shows the impact of GD-parameters variation (V_G and R_G) in the lifetime of PV-inverter devices.

At high $V_G=20$ V (low conduction losses), the R_G -variation has a negative impact of up to 50 % in device lifetime reduction from 20 years (GD with $V_G=20$ V and $R_G=7$ Ω) to 9.85 years (GD with $V_G=20$ V and $R_G=70$ Ω).

For a low V_G , the R_G -variation has a low impact (due to the very high conduction losses compared with switching losses) in devices lifetime, from 0.25 years (GD with $V_G=10$ V and $R_G=7$ Ω) to 0.2 years (GD with $V_G=10$ V and $R_G=70$ Ω).

Two main gate-driving operation points can be distinguished: the lowest loss operating point (V_{GS_max} and R_{G_min}) and the highest loss operating point (V_{GS_min} and R_{G_max}). According to the used GD-parameters, the device lifetime can vary with up to 100X times from 20 years (lowest loss operating point GD: $V_G=20$ V and $R_G=7$ Ω) to 0.2 years (highest loss operating point GD: $V_G=10$ V and $R_G=70$ Ω).

It can be concluded that the MP of the field where the PV-inverter is operating and the GD-parameter selection has a major impact in the converter devices reliability and it should be considered in the design stage to better optimize the

converter design margin. Therefore, a special attention has to be paid to the optimum GD-parameters selection for improving the lifetime of power-devices.

TABLE IV. GDS AND DEVICE DEGRADATION IMPACT IN LIFETIME

GD strategy (V_G, R_G)	Lifetime [years]		Degradation impact in lifetime
	Without Degradation	With Degradation	
1. GDs1 (20 V, 7 Ω)	26.41	20.06	28.2 %
2. GDs2 (17 V, 12 Ω)	13.16	10.2	29 %
3. GDs3 (15 V, 20 Ω)	5.6	4.3	30 %
4. GDs4 (14 V, 35 Ω)	3.41	2.6	31 %
5. GDs5 (12 V, 55 Ω)	1.72	1.3	32.4 %
6. GDs6 (10 V, 70 Ω)	0.268	0.2	34.1 %

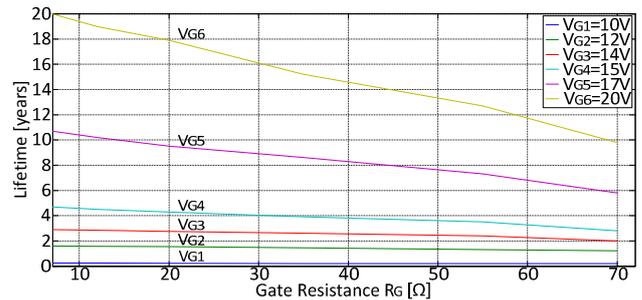


Fig. 12. GD-parameters (V_G and R_G) variation impact in PV-inverter devices lifetime

V. CONCLUSIONS

A reliability oriented design tool for the new generation of grid connected PV-inverters has been implemented. The detailed simulation model of the tool has been performed considering a real field mission profile model (for operating region Arizona, USA), a PV-panel model, a grid connected PV-inverter model, an Electro-Thermal model and the Lifetime model. The estimation of one-year thermal loading distribution of the converter devices (MOSFET, Diode) has been achieved and further used as an input to the lifetime model.

The proposed reliability oriented-design tool has been used to assess and study the impact of the MP-variation, GD-parameters variation and device aging-degradation in the PV-inverter devices lifetime.

The obtained results indicate that in order to improve the accuracy of the lifetime estimation, it is crucial to consider also the device degradation feedback in the simulation model, which has an impact of up to 34 % in the lifetime estimation for the studied case. Moreover, the MP of the field where the PV-inverter is operating and the GD-parameters selection, have an important impact in the converter reliability and it should be considered from the design stage, in order to avoid overdesign-underdesign of the product by choosing an optimum design margin in respect with the stress margin.

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